APPLICATION

FOR

UNITED STATES LETTERS PATENT

10059252 012902

TITLE: MEMORY CELL ARRAYS

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Express Mail Label No. EL858043837US:
Date: January 29, 2002

MEMORY CELL ARRAYS

CROSS REFERENCE TO RELATED APPLICATIONS

[001] This application is a continuation of U.S. Serial No. 09/340,983, filed June 28, 1999, which is a continuation-in-part of U.S. Serial No. 08/918,657, filed August 22, 1997, now U.S. Patent No. 6,025,221.

BACKGROUND

[002] The invention relates to memory cell arrays.

[003] In a continuing effort to reduce the size of memory devices, different memory cell array topologies have been proposed. Fig. 24 illustrates a portion of a typical memory cell array in a semiconductor memory device (such as a dynamic random access memory) that includes parallel word lines 100 running along one direction and bit lines 102 running generally perpendicularly to the word lines 100. Bit line contacts 104 electrically connect the bit lines 102 and the associated cell structure, generally indicated as 106.

[004] The size of each cell is typically described in terms of its feature size (F). The feature size is based on the width of the electrically conductive lines (i.e., the word lines and bit lines), referred to as L, and the width of the isolation space between the conductive lines, referred to as S. The sum of L and S is the minimum pitch of the memory device. The feature size (F) is half the minimum pitch, or half the sum of L and S, that is,

$$F = \frac{L+S}{2}. \qquad \text{(Eq. 1)}$$

[005] In the cell configuration shown in Fig. 24, the width of each cell along the word line direction is 2F while the width along the bit line direction is 4F. This results in a cell size of $8F^2$ (2Fx4F). To reduce the size of memory devices, reduced memory cell topologies have been proposed, including $6F^2$ cells. However, with reduced cell sizes, several issues need to be

addressed, including capacitor size, ease of contact to cells, and alignment between the contacts and cells.

[006] In addition, processing of semiconductor devices typically involves many steps in which layers of material are formed over a substrate and subsequently patterned into a desired feature or structure. Typical features or structures include conductive lines (e.g., word lines, bit lines) and contact openings. Each time a patterning or etching step is conducted, certain risks arise which can jeopardize the integrity of a wafer being processed. For example, a mask misalignment error can cause a subsequent etch to undesirably etch into wafer or substrate structure which can cause catastrophic failure. Accordingly, a need exists to reduce the number of processing steps utilized in the formation of integrated circuitry.

SUMMARY

[007] In general, in one embodiment, a memory device includes, bit lines and continuous active area lines extending generally in a first direction and intersecting at slanted portions.

[008] Other features and advantages will become apparent from the drawings and from the following claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[009] Figs. 1A and 1B are schematic diagrams of memory arrays.

[0010] Figs. 2A and 2B are enlarged, top views of a semiconductor wafer fragment in accordance with embodiments of the invention.

[0011] Fig. 3 is a cross sectional view of the Fig. 2A wafer fragment at one processing step taken along line 12-12 in Fig. 2A.

[0012] Fig. 4 corresponds to Fig. 3 but shows the wafer fragment at another processing step.

[0013] Fig. 5 corresponds to Fig. 3 but shows the wafer fragment at another processing step.

[0014] Fig. 6 corresponds to Fig. 3 but shows the wafer fragment at another processing step.

[0015] Fig. 7 corresponds to Fig. 3 but shows the wafer fragment at another processing step.

[0016] Fig. 8 corresponds to Fig. 3 but shows the wafer fragment at another processing step.

[0017] Fig. 9 corresponds to Fig. 3 but shows the wafer fragment at another processing step.

[0018] Fig. 10 corresponds to Fig. 3 but shows the wafer fragment at another processing step.

[0019] Fig. 11 corresponds to Fig. 3 but shows the wafer fragment at another processing step.

[0020] Fig. 12 corresponds to Fig. 3 but shows the wafer fragment at another processing step.

[0021] Fig. 13 is a cross-sectional view taken along line 19-19 in Fig. 3 after a processing step, which corresponds to the processing step shown in Fig. 8.

[0022] Fig. 14 corresponds to Fig. 3 but shows the wafer fragment at a processing step, which corresponds to the processing step shown in Fig. 10.

[0023] Fig. 15 corresponds to Fig. 3 but shows the wafer fragment at another processing step.

[0024] Fig. 16 corresponds to Fig. 3 but shows the wafer fragment at another processing step.

[0025] Fig. 17 corresponds to Fig. 3 but shows the wafer fragment at another processing step.

[0026] Fig. 18 corresponds to Fig. 3 but shows the wafer fragment at another processing step.

[0027] Figs. 19A and 19B correspond to Fig. 3 but show the wafer fragment at another processing step according to embodiments.

[0028] Fig. 20 is a slightly enlarged cross-sectional view taken along line 20-20 in Fig. 2A.

[0029] Fig. 21 is an enlarged top view of a semiconductor wafer fragment in accordance with another embodiment of the invention.

[0030] Fig. 22 is an enlarged top view of a semiconductor wafer fragment in accordance with another embodiment of the invention.

[0031] Fig. 23 is an enlarged top view of a semiconductor wafer fragment in accordance with another embodiment of the invention.

[0032] Fig. 24 is an enlarged top view of a conventional semiconductor wafer fragment.

DETAILED DESCRIPTION

[0033]In the following description, numerous details are set forth to provide an understanding of the present invention. However, it is to be understood by those skilled in the art that the present invention may be practiced without these details and that numerous variations or modifications from the described embodiments may be possible.

[0034] Fig. 1A is a schematic diagram of an exemplary memory array 20 in a memory device that includes word lines 26 running generally in parallel along one direction and bit line pairs 32 running generally in parallel along a perpendicular direction. A memory cell is represented schematically as a capacitor 8, and is connected by a transistor 9 to one of the bit lines BL. Each transistor 9 is activated by a word line 26.

[0035] A row of memory cells 8 is selected upon activation of a word line 26. The state of each memory cell in the row is transferred to a bit line 32 for sensing by the sense amplifiers 35, each connected to a pair of bit lines 32. In the illustrated embodiment, the bit lines 32 are vertically twisted at one or more predetermined locations in the array 20 to reduce soft error rates.

[0036] Fig. 2A shows the layout of a portion of the memory array of a semiconductor memory device according to one embodiment (which may be a dynamic random access memory or DRAM, for example). Other types of memory devices include synchronous DRAMs, video RAMs, or other modified versions of the DRAM. The memory array 20 includes a semiconductive substrate 22. As used in this document, the term "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including the "semiconductive substrates" described above.

[0037] The memory cell transfer transistors 9 are formed in the substrate 22 in a plurality of continuous active areas 24 running generally in parallel to each other. Each active area 24 is defined between isolation regions 34 (see Fig. 3) disposed relative to the substrate 22. To form a transistor in an active area, impurity doped regions (not shown) are formed in the substrate (along the length of each active area 24) to create the source and drain of the transistor. A word line 26 forms the gate of the transistor.

[0038] The transistor formed in the active area provides the pass gate that is controllable to electrically connect a cell capacitor (indicated as 102A, B, C, or D in Fig. 2A) to a bit line 32. Each of the capacitors 102 are electrically connected by contact plugs to an active area line 24 portion forming a node (source or drain) of a transistor 9. Each bit line 32 is connected to the active area line portion forming the other node of the transistor 9 by bit contact 100A or 100B. For example, activation of a word line 26C will cause the stored charges from the capacitors 102A and 102B to be transferred by corresponding transistors 9 to bit lines 32. Although depicted as squares in Fig. 2A, the contacts 100 can be of different shapes, and can take up the entire area of intersection between the bit lines 32 and the active area lines 24.

[0039] For clarity, each illustrated continuous active area line 24 has been shown to extend to outside of the boundary of substrate 22 utilizing dashed lines. Each individual active area is designated separately as 24', 24", and 24"'. To reduce the effective memory cell area while still maintaining ease of manufacture as discussed below, the continuous active areas 24', 24", and 24"' are not straight or linear, but rather weave relative to the substrate within which they are formed such that bends are created in each active area line 24 as it extends across the array. Effectively, the active area lines appear wavy across the array. The illustrated individual continuous active area lines extend generally horizontally across the page upon which Fig. 2A appears, but jog upwardly repeatedly as depicted in Fig. 2A to form protruding portions 19. This jogging is repeated along the length of the active area line 24.

[0040] Similarly, the bit lines 32 (which are formed above the active area lines 24) also weave relative to the substrate such that repeated depressed portions 21 are formed in the bit lines. The bit lines 32 run generally along the same direction as the active areas 24, but the direction of the jog in the bit lines 32 is opposite to the jog of the active area lines 24. Thus, in the Fig. 2A

embodiment, both bit lines and active area lines are formed to be wavy as they extend generally across the memory array. The bit lines and active area lines intersect at slanted portions 17 and 15, respectively, where the bit lines and active area lines are bent. In the Fig. 2A embodiment as well as in some other embodiments such as those described below, corresponding edges of the bit lines and active area lines are laterally spaced apart by some distance, that is, the bit lines and active area lines do not extend completely one on top of another except where they intersect at slanted portions.

[0041] Bit contacts 100 are formed at the intersections of the bit lines 32 and the active area lines 24. Since the bit lines 32 and active area lines 24 are slanted with respect to each other in the region of each intersection, formation of the contact hole in which the bit contact 100 is formed is made easier. This is because of the increase in width W of the contact hole (such as the contact hole 40 in Fig. 5) as compared to the width if both the active area lines 24 and bit lines 32 are generally straight. As the feature size of memory devices continue to decrease (e.g., 0.18 or 0.25 microns), such increases in the width of the bit contact holes result in generally more reliable bit contacts.

[0042] More specifically, as depicted in Fig. 2A, each of the bit lines 32 and active area lines 24 run generally along the X direction. The jogs in the bit lines and active area lines are formed at predetermined positions A-A, B-B, C-C, and D-D. At position A-A, each active area line 24 bends or jogs in a first direction (e.g., upwards) while each bit line 32 bends or jogs in a second, opposite direction (e.g., downwards). The angle of the bends can be set at, for example, about 22.5°, although other angles are also possible. In addition, the directions of the active area and bit lines bends or jogs can be switched.

[0043] As further shown in Fig. 2A, at position B-B, each of the active area and bit lines bends or jogs back in the opposite directions of the corresponding bends or jogs at position A-A such that both the active area and bit lines run again generally along the X direction. At position C-C the active area and bit lines bend or jog again, also in the opposite directions from the corresponding bends or jogs at position A-A. At position D-D, the lines bend or jog back to run generally in the X direction.

[0044] One advantage of weaving both the active area and bit lines in the array is that a smaller bend angle is required for the repeated jogs while still achieving the desired memory cell area reduction.

[0045] Further, if desired, the amount of bending of the active area and bit lines can be selected to be different. Thus, for example, the angle of the bends in each active area line can be selected to be larger than the angle of the bends in each bit line. This may be desirable since it is easier to form the deeper jogs in the active area lines since they are formed in a relatively flat surface of the substrate as compared to the bit lines, which are formed over a number of structures, including word lines.

[0046] A plurality of conductive lines 26, 28 are also formed (under the bit lines 32) that run generally perpendicularly to the active area 24 and bit lines 32. In the illustrated example, four of the conductive lines are designated with numeral 26 and one of the conductive lines is designated with numeral 28. A pair of conductive lines 26 may be seen on either side of conductive line 28. The conductive lines 26 form the access or word lines (or access gates) in the DRAM array, while the conductive lines 28 are grounded to provide isolation lines (or isolation gates) between word lines 26. Conductive lines 26, 28 run generally vertically as viewed in Fig. 2A. The active area lines 24 and conductive lines 26, 28 constitute or define an array over which a plurality of memory cells are formed.

[0047] In the array 20, the word or access lines 26 are relatively straight (formed generally as parallelograms in given portions of the array). The word or access lines 26 intersect slanted portions of the active area lines 24 and bit lines 32.

[0048] The area which is consumed by a single memory cell in accordance with this embodiment is illustrated by dashed outline 30. Such area can be considered or described as relative to the feature size F, as discussed above. As shown, a single memory cell is about 3F wide by about 2F deep, thus providing a consumed area for a single memory cell of about $6F^2$. In one implementation, F is no greater than 0.25 micrometer, and preferably, no greater than 0.18 micrometer. However, other dimensions (either larger or smaller) are also contemplated.

[0049] In one implementation, adjacent word lines 26 share an intervening bit contact 100 of adjacent pairs of memory cells as will become apparent below. For example, as shown in Fig. 2A, word lines 26C and 26D share bit contacts 100A and 100B, while word lines 26A and 26B share bit contacts 100C and 100D. Electrical isolation between the adjacent pairs of memory cells is provided by intervening isolation line 28. Line 28, in operation, is connected with a ground or suitable negative voltage. Alternatively, the electrical isolation can be provided by field oxide.

[0050] Bit contacts 100, which can be formed of an electrically conductive plug 46 (as shown in Fig. 12) and can be made of a conductively doped polysilicon, electrically connect the bit lines 32 to the underlying active areas 24. The bit contacts 100 are located in the space 104 between two adjacent word lines 26. The memory cell capacitors 102 are electrically contacted to the active areas 24.

[0051] The Fig. 2B embodiment is the same as the Fig. 2A embodiment except that bit contacts 101 (101A, 101B, 101C, and 101D illustrated) in the Fig. 2B embodiment are formed with a different process than bit contacts 100 (100A, 100B, 100C, and 100D) in the Fig. 2A embodiment. Similarly, formation of contacts from electrodes of capacitors 102 to corresponding active areas 24 is also different. This is described further below.

[0052] According to one embodiment, cross-sectional views of the memory array 20 of Fig. 2A are shown in Figs. 12 and 19A, which are cross-sections taken along lines 12-12 and 19-19, respectively. In Fig. 12, active areas 24 are defined relative to the substrate 22, with the bit contacts 100, which include electrically conductive plugs 46, disposed above and in electrical contact with portions of the active areas 24. Further, the bit lines 32, which can be formed of electrically conductive multilayer structures 56, are disposed above and in electrical contact with the bit line contact plugs 46.

[0053] In Fig. 19A, the cell capacitors 102 are illustrated. Fig. 19B illustrates an alternative embodiment, as described below. Each capacitor 102 is formed of a first capacitor plate 64, a dielectric layer 66, and a second capacitor plate 68. The first capacitor plate 64 of each cell is electrically contacted to the plug 46 for electrical connection to the active area 24. The cell

capacitor structure is laid over the bit line structure 56, which forms a cell-over-bit line (COB) array structure. An advantage the COB structure offers is that bit line contact openings need not be made in the second capacitor plate 68, which eliminates difficulties associated with aligning bit line contact openings in the second plate 68 to cell structures or word lines in the array. The bit line structure 56 is referred to as a buried bit line and corresponds to the bit line 32 in Fig. 2A.

[0054] Although Figs. 12 and 19A illustrate details of cross-sections of the memory array according to one embodiment, it is to be understood that the invention is not to be limited in this respect. Other types of memory structures are contemplated and within the scope of the present invention.

[0055] In the illustrated embodiment, a "double deck" bit line architecture is used, which includes the buried bit line 56 and a top deck bit line 33 (Figs. 12 and 19A) formed above the buried bit lines 32 and the capacitors 102. As shown in Figs. 12 and 19A, an insulating layer 39 is formed between the top deck bit line 33 and the underlying structure. The top deck bit line 33 is generally formed of a metal, such as aluminum. In Fig. 1A, the top deck bit line 33 is represented schematically as solid lines, while the buried bit lines 32 are represented as dashed lines. The top deck bit lines 33 do not make contact with the memory array. Contact to the memory array transistors are made by the buried bit lines. At the locations where twists are indicated (such as vertical twists 29 and 31 in Fig. 1A), the top deck bit line 33 is connected to a buried bit line 32. Because the top deck bit lines 33 do not need to make contact to the underlying cell structure, they can be relatively straight, as shown in Figs. 12 and 19A. In addition, contact openings are not needed through the second capacitor plate 68 (Fig. 19A) of the memory array. This avoids problems associated with aligning the contact openings in the second capacitor plate 68 to the underlying word line and bit line structures.

[0056] By using the double deck bit line structure, the bit lines 32, 33 can be connected to the sense amplifiers 35 in a vertically folded bit line configuration, as depicted in Fig. 1A. Thus, with the double deck bit lines in a vertically folded bit line arrangement, the column pitch occupies a 2F width, as opposed to a 4F pitch for traditional memory cells. This allows formation of a $6F^2$ memory cell. One advantage of the folded bit line configuration is that it is

less susceptible to soft errors than the open bit line configuration. Because a bit line pair is connected to each sense amplifier 35 on the same side of the sense amplifier, noise created by alpha particles will couple to both of the bit lines in the pair. As the sense amplifier 35 detects the difference in voltage between the pair of bit lines, errors due to such noise effects are reduced. In an alternative embodiment, the $6F^2$ memory cell may be used with an open bit line arrangement, in which BL and BL_ are on opposite sides of a sense amplifier, as illustrated in Fig. 1B.

[0057] Referring to Fig. 21, an alternative embodiment of an array containing reduced size memory cells (e.g., $6F^2$ cells) is shown. In this configuration, bit lines 200 are formed to weave relative to the substrate 20, while continuous active area lines 202 are generally straight. Bit contacts 206 are formed at the intersections between the bit lines 200 and active area lines 202. In addition, memory cell capacitors 208 are formed over and are in electrical contact with portions of the active area lines 202. Although illustrated as generally straight it is to be understood that the straightness of the active area line or other structures (including bit lines) in this application depends on manufacturing tolerances. In addition, slight protrusions may be needed for forming contacts or other structures.

[0058] As illustrated, each bit line 200 runs generally in the X direction and jogs or protrudes upwardly in a repeated pattern. Each bit line 200 bends upwardly at position A-A (at an angle of about 45° with respect to the X axis). The bit line 200 then bends in the opposite direction at position B-B so that it runs generally in the X direction. After a short run, the bit line 200 then bends downwardly at position C-C. At position D-D, the bit line 200 again bends back to run generally in the X direction. This pattern is repeated throughout the memory array to provide a wavy bit line.

[0059] As indicated by the dashed outline 210, the feature size of the memory cell in this configuration is also about $6F^2$ (3F by 2F). Conductive lines 204, 205 run generally perpendicularly to the active areas 202. The conductive lines 204 form the word lines in the array while the lines 205 are grounded or driven to a negative voltage to provide electrical isolation between word lines 204.

[0060] In comparing the memory cell layouts shown in Figs. 2A and 21, one advantage offered by the cell layout of Fig. 2A is that photolithography exposure to form the bit lines and active areas is easier to achieve due to the smaller bends of the bit lines and active areas in the Fig. 2A embodiment.

[0061] Referring to Fig. 22, an alternative memory cell configuration is illustrated. In this configuration, the bit lines 300 are generally straight while the active area lines 302 weave relative to the bit lines. In this embodiment, the continuous active areas 302 run generally in the X direction and have repeated downward jogs. Creating weaving continuous active areas can be simpler than creating weaving bit lines. Active areas are defined by isolation regions relative to a substrate, which initially is on a flat surface of a wafer. Because of the flatness, the bends in the active areas do not create as many photolithographic difficulties as with bit lines, which generally run over relatively rough terrain since the bit lines make contact to the active area surface in some portions and are isolated from active areas in other portions (where the cell capacitors are formed).

[0062] At position A-A, the active area lines 302 bend at an angle of about 45°, then bend back at position B-B to run in the X direction. At position C-C, the active area lines bend in the opposite direction from the A-A bend, and bend back to run in the X direction again at position D-D. This pattern is repeated throughout the array.

[0063] Bit line contacts 306 are defined at the intersection regions of the bit lines 300 and active areas 302, and memory cell capacitors 310 are formed over portions of the active area 302 for connection to the bit lines in response to activation of a word line. Again, the effective memory cell area is $6F^2$, as indicated by the dashed outline 310.

[0064] Referring to Fig. 23, a staggered, weaving bit line configuration is illustrated. In this configuration, continuous active area lines 402 are straight while bit lines 400 (which run generally in the X direction) are bent at predefined positions. The bit lines 400 are staggered because they continue to bend in the same direction and do not bend back as in the configuration of Fig. 22. At position A-A, the bit lines 400 bend in a first direction by about 45°, then bend back at position B-B to run in the X direction. At position C-C, the bit lines 400 bend again in

the first direction, and bend back at position D-D. This is repeated throughout the array. Because the bit lines are so staggered, the entire array needs to be staggered to accommodate the generally diagonal direction of a column in the array. As a result, the array ends up being generally trapezoidally shaped.

[0065] Running generally perpendicularly to the active area lines 402 are conductive lines 404, 405. The conductive lines 404 are word lines, while the conductive line 405 is grounded or negatively biased to provide isolation.

[0066] Thus, in the embodiments described, either the bit lines or active area lines, or both, may be weaved by bending the lines at predetermined locations. As examples, the bends in the bit lines and active area lines may range between about 15° and 60°, although larger or smaller angles may be possible with other embodiments.

[0067] Embodiments of the invention may have one or more of the following advantages. The memory array size can be reduced while not significantly increasing the complexity of the fabrication process. Ease of contact from the bit lines to a node in the memory cell is maintained even though memory cell size is reduced. The cell provides a larger area for the capacitor container, thereby reducing the stack height and the vertical height of the bit line contact. No contacts are necessary in the memory array, thereby making contact-to-cell plate alignment easier.

[0068] Turning now to Figs. 3-12, a view is taken along line 12-12 in Fig. 2A at a processing point which is prior to the Fig. 2A construction. Although process steps according to one embodiment are illustrated in Figs. 3-20, it is to be understood that the invention is not to be restricted to such a process of manufacturing embodiments of the invention. The manufacturing process may be modified and structures may be different in further embodiments.

[0069] Referring to Fig. 3 a plurality of isolation oxide regions 34 are disposed relative to substrate 22. Regions 34 define, therebetween, continuous active areas 24. Individual continuous active areas 24', 24", and 24"' are indicated in their corresponding positions relative to the Fig. 2A construction. A first insulative layer of material 36 is formed over substrate 22 and the array of continuous active areas 24. The first insulative layer is also formed over

conductive lines 26, 28 (Fig. 2A). Insulative layer 36 has an upper surface 37. An exemplary material for layer 36 is borophosphosilicate glass.

[0070] Referring to Fig. 4, a masking material layer or masking substrate such as photoresist is formed over substrate 22 and patterned to form blocks 38. The patterning of the masking material layer provides a single mask which defines a plurality of patterned openings which are designated at 40(42). The significance of the parenthetical designation is to indicate that openings 40(42) are formed and collectively arranged to define a pattern of both bit line contact openings 40 and capacitor contact openings 42. Accordingly, both capacitor contact openings and bit line contact openings are patterned over insulative layer 36 in a common masking step.

[0071] Referring to Fig. 5, openings are etched or otherwise formed in or through first insulative layer 36 to expose active area portions corresponding to the illustrated active areas 24. The exposing of the active area portions defines both capacitor contact openings 42 and bit line contact openings 40 for memory cells 30 (Fig. 2A) which are to be formed. In accordance with an embodiment, both the capacitor contact openings and the bit line contact openings are etched at the same time. Such openings, however, can be etched at different times. The pattern which defines the layer 36 material to be etched or removed may be a stripe that follows the corresponding continuous active areas 24. Blocks 38 are then stripped or otherwise removed. In one aspect, the stripping or removal of blocks 38 constitutes removing photoresist proximate the patterned bit line contact openings and capacitor contact openings in at least one common step.

[0072] In an alternative embodiment, instead of a stripe pattern to form bit contacts 100 and capacitor cell contacts, a process may form individual contact holes to form bit contacts 101 and capacitor cell contacts. As illustrated in Fig. 2B, the holes formed for bit contacts 101 may be made to be slightly oversized to account for potential misalignment. As a result, some overlap of the contact holes and the conductive lines 26 and 28 (word lines and isolation lines) may occur. The capacitor cell contacts may also be made slightly oversized to ensure alignment.

[0073] Referring to Fig. 6, a layer 44 of conductive material is formed over substrate 22 and the memory array. The layer 44 may be formed within both the capacitor contact openings and the illustrated bit line contact openings 40 of Fig. 5. Such material may be in electrical communication with the associated active area portions over which it is formed. An exemplary material for layer 44 comprises conductively doped polysilicon.

[0074] Referring to Fig. 7, portions of the layer 44 are removed to a degree sufficient to electrically isolate conductive material plugs 46 within the openings defined by first insulative layer 36. The removal of layer 44 material can be accomplished by any suitable method which is effective to isolate the illustrated plugs 46. Such can include a resist etch back, a timed etch, or planarization relative to upper surface 37 of insulative layer 36. In accordance with an embodiment of the invention, layer 44 material is selectively removed relative to the insulative layer and to a degree sufficient to recess the conductive material below the insulative layer upper surface 37. Such removal effectively forms isolated conductive material plugs 46 within the individual associated openings. Recessed conductive plugs 46 are shown in Fig. 13 and correspond to conductive plugs which are formed relative to and within capacitor contact openings 42. All of such plugs of conductive material may be in electrical communication with their associated substrate portions 24.

[0075] Referring to Figs. 8 and 13, a layer 48 of second insulative material is formed over the array and over all of the previously formed conductive plugs. Accordingly, layer 48 material is formed over and relative to bit line contact openings 40 and capacitor contact openings 42 (Fig. 13). An exemplary material for layer 48 is SiO_2. Other insulative materials can be used, such as silicon nitride.

[0076] Referring to Figs. 9 and 13, material of second insulative layer 48 is removed from only over bit line contact openings 40 (Fig. 9) to expose the associated plugs 46. Such can be accomplished by a suitable masked etch of the second insulative layer material from over bit line contact openings 40. Accordingly, as shown in Fig. 13, material of insulative layer 48 remains over the plugs 46 which are disposed within the capacitor contact openings 42. This effectively electrically insulates the associated capacitor contact opening plugs during formation of buried bit or digit lines described below.

[0077] Referring to Figs. 10 and 14, various layers of material from which buried bit lines are to be formed are formed over the substrate. In one implementation, a layer 50 of conductive material is formed over substrate 22. As shown in Fig. 10, layer 50 is in electrical communication with plugs 46. However, as shown in Fig. 14, layer 50 is electrically insulated from plugs 46 by second insulative material layer 48. An exemplary material for layer 50 is conductively doped polysilicon. A more conductive layer 52 (containing silicide, for example) can be provided over layer 50. An exemplary material for layer 52 is WSi_x or W. A layer 54 of insulative material can be formed over layer 52. An exemplary material for layer 54 is an oxide material. The above constitutes but one way of forming the layers which comprise the bit lines. Other materials and layers are possible.

[0078] Referring to Figs. 11 and 15, such layers are subsequently patterned and etched to define a plurality of bit lines 32 having conductive bit line portions 56 which, as shown in Fig. 11, are in electrical communication with respective plugs 46. However, as shown in Fig. 15, bit lines 32 are disposed over first insulative layer 36 and electrically insulated from the corresponding conductive plugs 46 by layer 48. This constitutes one way of forming a plurality of conductive bit lines over the array with individual bit lines being operably associated with individual continuous active areas and in electrical communication with individual respective plugs of conductive material within the bit line contact openings 40 (Fig. 11).

[0079] Referring to Figs. 12 and 16, a layer 58 of insulative spacer material is formed over the substrate as shown. Such material can comprise either a suitable oxide or nitride material. In one implementation, layer 58 comprises an oxide formed through suitable decomposition of tetraethyloxysilicate (TEOS). Such effectively electrically insulates exposed conductive portions 56 of the conductive bit lines.

[0080] Referring to Fig. 17, a third insulative layer 60 is formed over the array. An exemplary material for layer 60 is borophosphosilicate glass (BPSG).

[0081] Referring to Fig. 18, layer 60 material is patterned and etched over and relative to conductive plugs 46 and capacitor contact openings 42 to expose the associated conductive

plugs. Accordingly, such forms capacitor openings 62 within which capacitors are to be formed.

[0082] Referring to Fig. 19A, individual first capacitor plate structures 64 are formed relative to and within associated capacitor openings 62. Such plate structures are in electrical communication with individual respective plugs 46. A layer 66 of dielectric material and second capacitor plate structure 68 are formed relative to and operably associated with individual first capacitor plate structures 64 to provide individual memory cells which, in accordance with one embodiment, form DRAM storage capacitors. The insulating layer 39 may be formed in the opening 42 (defined by the wall of the second capacitor plate 68) as well as above the capacitor. In an alternative embodiment, as shown in Fig. 19B, a plug 43 (formed of polysilicon or other conductive material, for example) may be formed in the opening 42 to fill up the opening at about the same level as the layer 54. Alternatively, the plug 43 may be formed below the level of the layer 54 (to provide a recessed plug) or above the level of the layer 54 (to provide individual plugs). The plug 43 is defined between isolation spacers 73 surrounding the bit lines 32. An advantage of such an embodiment is that a deep self-aligned contact (SAC) etch to open up the hole 42 can be avoided in order to contact the layer 46.

[0083] In an alternative embodiment, instead of using a memory cell capacitor in a container as shown in Figs. 19A and 19B, a stud, a protruding solid plug, or other structure protruding generally upwardly can be formed so that the outer surface of the protruding structure is used to provide the surface area of the capacitor. This enhances the cell capacitance as dimensions continue to shrink, which may limit the surface area available with container-shaped capacitors.

[0084] Referring to Fig. 20, an enlarged view of the array taken generally along line 20-20 (Fig. 2A) is shown. The section is taken along a buried bit line 32. Accordingly, as shown, bit line 32 may be seen to overlie conductive lines 26, 28 and associated isolation oxide regions 34. Bit line 32 can also be seen to be in electrical communication with the two illustrated plugs 46 that act as bit line contacts.

[0085] The above described methodology may have advantages over prior processing methods. One such advantage is that both the bit line contact openings and the capacitor contact openings are patterned in a common masking step. Hence, bit line contacts and capacitor contacts can be formed at the same time. Accordingly, processing steps are reduced. Additionally, extra processing steps which were formerly necessary to remove undesired conductive material left behind after bit line formation may be reduced, if not eliminated. Furthermore, bit line-to-word line capacitance may be reduced.

[0086]While the invention has been disclosed with respect to a limited number of embodiments, those skilled in the art will appreciate numerous modifications and variations therefrom. It is intended that the appended claims cover all such modifications and variations as fall within the true spirit and scope of the invention.

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